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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/435,154	11/08/1999	SHUNPEI YAMAZAKI	SEL142	4834

7590 10/07/2003

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EXAMINER	
LOKE, STEVEN HO YIN	
ART UNIT	**PAPER NUMBER**
2811	

DATE MAILED: 10/07/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/435,154	YAMAZAKI ET AL.	
	Examiner	Art Unit	
	Steven Loke	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 July 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,6-9,11,12,14-17,19-22,24 and 25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,6-9,11,12,14-17,19-22,24 and 25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-4, 6-9, 14-17 and 19-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki et al. (U.S. patent no. 6,274,887).

In regards to claims 1, 6, 14, 19, Yamazaki et al. disclose a goggle type display having a liquid crystal display (LCD) device having a CMOS circuit comprising an n-channel TFT and a p-channel TFT in figs. 1, 2A-5B, 12 and 13D. The CMOS circuit comprising: each gate electrode of the n-channel TFT and the p-channel TFT having a first conductive layer (the inner sub-layer of each of the gate electrodes [107, 113]) (see also the blue portion of each of the gate electrodes [107, 113] in Attachment A) being in contact with a gate insulating film [106, 112], and a second conductive layer (the outer sub-layer of each of the gate electrodes [107, 113]) (see also the red portion of each of the gate electrodes [107, 113] in Attachment A) being in contact with the gate insulating film and top and side surfaces of the first conductive layer; a semiconductor layer of the n-channel TFT comprising a first channel formation region [102], a pair of LDD regions [103] and first source and drain regions [105]; and a semiconductor layer of the p-channel TFT comprising a second channel formation region [110] and second source and drain regions [111], wherein a portion which the second conductive layer is in contact with the gate insulating film in the n-channel TFT partially overlaps the pair of LDD regions; wherein the portion which the second conductive layer is in contact with

the gate insulating film in the n-channel TFT does not overlap the first source and drain regions; wherein a portion which the second conductive layer is in contact with the gate insulating film in the p-channel TFT is partially overlaps the second source and drain regions, wherein the semiconductor layer of the p-channel TFT has no LDD regions.

Yamazaki et al. differ from the claimed invention by not showing the liquid crystal is ferroelectric liquid crystal. It would have been obvious for the liquid crystal is ferroelectric liquid crystal, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use. In re Leshin, 125 USPQ 416.

It is inherent that each of the gate electrodes of the n-channel TFT and the p-channel TFT comprising a first conductive layer and a second conductive layer because a single conductive layer always comprises a plurality of sub conductive-layers. Therefore, Yamazaki et al. disclose a first conductive layer (the inner sub-layer of each of the gate electrodes [107, 113]) and a second conductive layer (the outer sub-layer of each of the gate electrodes [107, 113]) for each of the gate electrodes [107, 113] of the n-channel TFT (NTFT) and the p-channel TFT (PTFT).

In regards to claims 2, 7, 15, 20, Yamazaki et al. further disclose the first conductive layers of the n-channel TFT and the p-channel TFT comprise tantalum (col. 10, lines 53-55).

In regards to claims 3, 8, 16, 21, Yamazaki et al. further disclose each of the first conductive layers of the n-channel TFT and the p-channel TFT comprises a single layer.

In regards to claims 4, 9, 17, 22, Yamazaki et al. further discloses the second conductive layers of the n-channel TFT and the p-channel TFT comprise tantalum (col. 10, lines 53-55).

3. Applicant cannot rely upon the foreign priority papers to overcome the above rejection because a translation of said papers has not been made of record in accordance with 37 CFR 1.55. See MPEP § 201.15.

4. Claims 11-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miyasaka et al. (U.S. patent no. 6,180,957).

In regards to claim 11, Miyasaka et al. disclose a liquid crystal display device having an n-channel TFT and a p-channel TFT over a substrate in figs. 26, 49A, and 49B. It comprises: an n-channel TFT comprising: a first gate electrode formed adjacent to a first semiconductor layer with a first gate insulating film [5] interposed therebetween, the first semiconductor layer comprising a first channel formation region [2], a pair of LDD regions [9] and first source and drain regions [3]; wherein the first gate electrode partially overlaps the pair of LDD regions [9]; and the p-channel TFT comprising: a second gate electrode [6] formed adjacent to a second semiconductor layer with a second gate insulating film interposed therebetween, the second semiconductor layer comprising a second channel formation region and second source and drain regions [4, 10] being in contact with the second channel formation region, wherein the second gate electrode [6] partially overlaps the second source and drain regions [4, 10], and a wiring [8] is connected to at least one of the second source and drain regions [4, 10].

Miyasaka et al. differ from the claimed invention by not showing the liquid crystal is ferroelectric liquid crystal. It would have been obvious for the liquid crystal is ferroelectric liquid crystal, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use. In re Leshin, 125 USPQ 416.

In regards to claim 12, Miyasaka et al. differ from the claimed invention by not showing the first and second gate electrodes comprise a material selected from the group consisting of titanium, tantalum, tungsten and molybdenum. It would have been obvious for the first and second gate electrodes comprise a material selected from the group consisting of titanium, tantalum, tungsten and molybdenum, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use. In re Leshin, 125 USPQ 416.

5. Claims 24-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miyasaka et al. (U.S. patent no. 6,180,957) as set forth in the rejection of claim 11, further in view of Johnson.

In regards to claim 24, Miyasaka et al. further differ from the claimed invention by not showing the CMOS circuit is used in a goggle type display device.

Johnson shows a goggle type LCD display device having a control circuitry and a display screen [12] in figs. 1 and 2.

Since Miyasaka et al. and Johnson teach a LCD device with control circuitry, it would have been obvious to have the CMOS circuit of Miyasaka et al. in the control circuit of Johnson because it increases the speed of the device.

In regards to claim 25, the combined device differs from the claimed invention by not showing the first and second gate electrodes comprise a material selected from the group consisting of titanium, tantalum, tungsten and molybdenum. It would have been obvious for the first and second gate electrodes comprise a material selected from the group consisting of titanium, tantalum, tungsten and molybdenum, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use. In re Leshin, 125 USPQ 416.

6. Applicant's arguments filed 7/17/03 have been fully considered but they are not persuasive.

It is urged, in page 11 of the remarks, that Yamazaki et al. contain no disclosure or suggestion of the alleged "outer" and "inner" sub-layers and there is nothing in Yamazaki et al. defining the boundary between the alleged outer sub-layer and the alleged inner sub-layer. However, as mentioned in the rejection and the Attachment A, it is inherent that each of the gate electrodes of the n-channel TFT and the p-channel TFT of Yamazaki et al. comprising a first conductive layer (the blue portion of each of the gate electrodes [107, 113] in Attachment A) and a second conductive layer (the red portion of each of the gate electrodes [107, 113] in Attachment A) because a single gate conductive layer always comprises a plurality of sub gate conductive layers. Therefore, Yamazaki et al. disclose a first conductive layer (the inner sub-layer of each of the gate electrodes [107, 113]) (the blue portion of each of the gate electrodes [107, 113] in Attachment A) and a second conductive layer (the outer sub-layer of each of the gate electrodes [107, 113]) (the red portion of each of the gate electrodes [107, 113] in

Attachment A) for each of the gate electrodes [107, 113] of the n-channel TFT (NTFT) and the p-channel TFT (PTFT). In addition, Yamazaki et al. further disclose the portion (the red portion of the gate electrode [113] in Attachment A) which the second conductive layer is in contact with the gate insulating film [112] in the p-channel TFT partially overlaps the second source and drain regions [111] as recited in the claimed invention.

It is urged, in page 6 of the remarks, that region 10 in Fig. 26 in Miyasaka et al. appears to be a LDD region (Llddp), not a source or drain region, as required in the claim. In addition, Miyasaka et al. also urged that the source and drain regions [3, 4] and the LDD regions [9, 10] have different impurity concentrations. However, a LDD (lightly doped drain) region is also considered as a drain region. Since the claimed invention never discloses the source and drain regions having a higher impurity concentration than the LDD regions, region [10] of Miyasaka et al. is also considered as a source or drain region. Therefore, the source and drain regions [10] in Miyasaka are in contact with the channel region, as required in the Claim 11. Miyasaka et al. meet the limitation of the claimed invention.

It is urged, in page 12 of the remarks, that independent claim 24 and those claims dependent thereon are not disclosed or suggested by the cited references because of the reasons discussed for Claim 11. Since Miyasaka et al. is still read on claim 11, the combination of Miyasaka et al. and Johnson is still read on claim 24 and its dependent claim.

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven Loke whose telephone number is (703) 308-4920. The examiner can normally be reached on 7:50 am to 5:20 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (703) 308-2772. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

sl
October 2, 2003

Steven Loke
Primary Examiner
Steven Loke

Attachment A

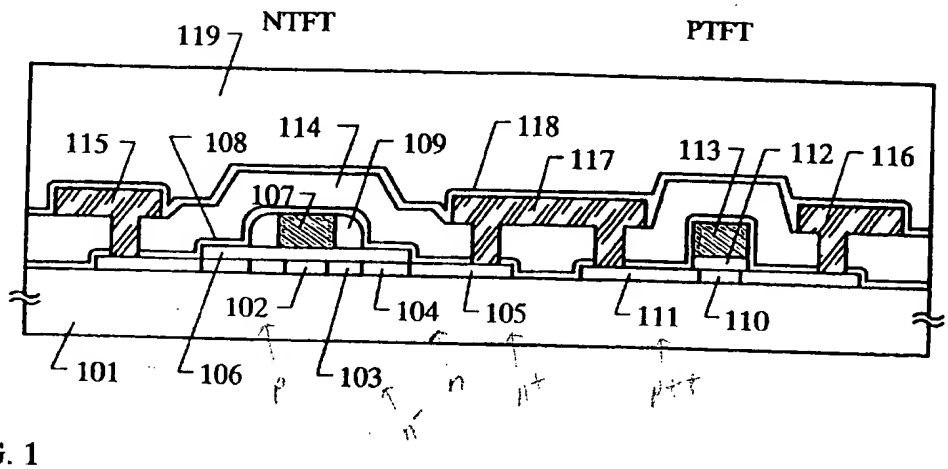

FIG. 1

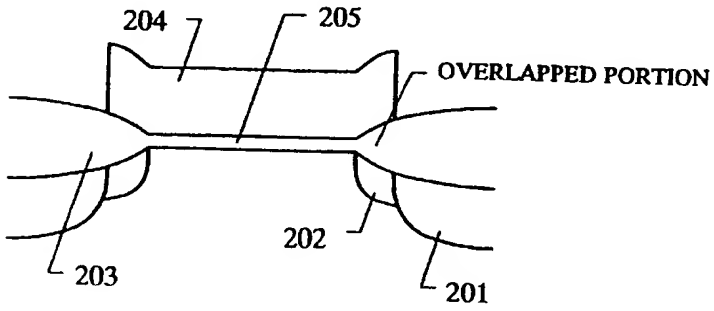

FIG. 2A

PRIOR ART

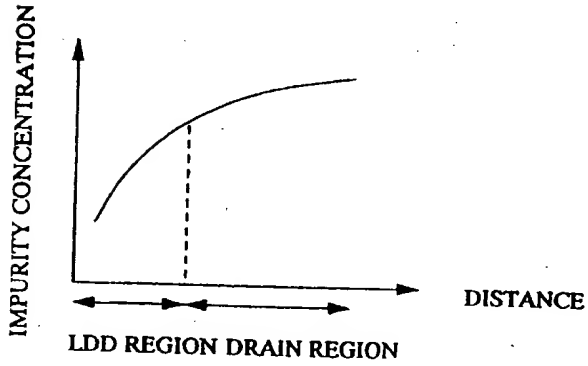

FIG. 2B

PRIOR ART